

UNITED STATES PATENT APPLICATION

FOR

FLIP-CHIP OPTO-ELECTRONIC CIRCUIT

INVENTORS:
JUN SU

PREPARED BY:

CHARLES K. YOUNG
INTEL CORPORATION
2200 MISSION COLLEGE BLVD.
SANTA CLARA, CA 95052-8119

(408) 765-8080

Attorney's Docket No. 42390.P13376

Express Mail" mailing label number EL821772347US

Date of Deposit: December 27 2001

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: U.S. Patent and Trademark Office, Post Office Box 2327, Arlington, VA, 22202

Raquel R. Torres
(Typed or printed name of person mailing paper or fee)

Raquel R. Torres
(Signature of person mailing paper or fee) Date

FLIP-CHIP OPTO-ELECTRONIC CIRCUIT

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The described invention relates to the field of opto-electronic circuits. In particular, the invention relates to an opto-electronic circuit that is coupled to a package substrate via solder bump technology.

10

2. Description of Related Art

Optical circuits include, but are not limited to, light sources, detectors and/or waveguides that provide such functions as multiplexing, demultiplexing and/or switching. Planar lightwave circuits (PLCs) are optical circuits that are

15 manufactured and operate in the plane of the circuit. PLC technology is advantageous because it can be used to form small-scale components, such as array waveguide grating (AWG) filters, optical add/drop (de)multiplexers, optical switches, monolithic, as well as hybrid opto-electronic integration devices. Such devices formed with optical fibers would typically be much larger. Further, PLC
20 structures may be batch fabricated on a silicon wafer.

An opto-electronic device circuit combines both electrical and optical functions. One type of opto-electronic circuit is a thermo-optic switch (TOS) made of a Mach-Zehnder interferometer. In a TOS, an optical signal is switched by providing an electrical input, i.e., an electrical current, to heat a heating element

PCT/US2019/033766

adjacent to an optical waveguide made of material, such as silica-on-silicon, that is sensitive to temperature. Heating the temperature-sensitive optical waveguide changes the refractive index and controls the path length of the optical waveguide, which results in the optical signal switching its optical path in the TOS, as is well-known.

5 Various types of thermo-optic switches have been commercialized, such as 1x1, 1x2, 2x2, 4x4, 8x5 and 8-arrayed 2x2 varieties.

An opto-electronic device, such as a thermo-optic switch is typically coupled to an external electrical power supply by wire bonding from the power supply to the heating element of the thermo-optic switch.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram showing one embodiment of an opto-electronic circuit.

5 Figure 2 is a schematic diagram showing an example of a cross-section of an opto-electronic device attached to a circuit board.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

DETAILED DESCRIPTION

An opto-electronic circuit is coupled to a package substrate through solder bumps. The solder bumps provide electrical connections to the opto-electronic circuit. In one embodiment, solder bumps are coupled to heating elements of a thermo-optic switch (TOS).

Figure 1 is a schematic diagram showing one embodiment of an opto-electronic circuit. In this embodiment, a TOS 105 is fabricated on a first substrate 100. A first heating element 110 is coupled to one portion of the TOS 105, and a second heating element 112 is coupled to a second portion of the TOS 105. In one embodiment the heating elements 110, 112 are applied in a process step that leaves the heating elements 110, 112 at least partially exposed on a top surface of the first substrate 100. The substrate 100 is subsequently turned upside down for coupling to the package substrate 150.

The package substrate 150 comprises multiple conductive strips, such as conductive strips 151, 152, and 153. The conductive strips 151, 152, and 153 are designed to make electrical contact with the exposed conductive surfaces of the TOS 105, such as the heating elements 110, 112. In one embodiment the TOS 105 is coupled to the package substrate 150 at the conductive strips 151, 152, and 153 via solder bump technology.

Solder bump technology, also called flip-chip or control collapse chip connection (“C4”) technology, uses solder bumps to both attach and establish electrical connections to a package substrate 150. With this technology, solder

PCT/US2017/038272

bumps are reflowed to make connection to terminal pads on the package substrate 150.

In the example of Figure 1, one end of the heating elements 110, 112 makes contact with conductive strips 151 and 152, respectively, and the other end of the 5 heating elements 110, 112 makes contact with conductive strip 153 as a “common”, which in one embodiment may be coupled to a common ground.

In one embodiment, the conductive strips 151, 152, 153 are coupled to conductive pads 161, 162, 163, respectively, on an opposite side of the package substrate through vias 171, 172, 173, respectively. The conductive pads 161, 162, 10 163 are coupled to leads or solder bumps for attaching the package substrate to a circuit board. Additionally the conductive pads 161, 162, 163 may assist with heat dissipation from the TOS 105.

Figure 2 is a schematic diagram showing an example of a cross-section of an opto-electronic device 200 attached to a circuit board 220. An opto-electronic 15 substrate 205 is coupled to a package substrate 210 via solder bump technology comprising conductive pads 230 on the opto-electronic substrate, solder bumps 232, and conductive strips 234 on the package substrate 210.

In one embodiment, the conductive strips 234 of the package substrate 210 are coupled to conductive pads 240 on the opposite surface of the package substrate 20 210, and the conductive pads 240 are attached to the circuit board 220 via solder bumps 242. Alternatively, the conductive strips 234 of the package substrate may be coupled to leads for attaching the package substrate 210 to a circuit board 220. In

4567891011121314

one example, the leads may be surface mountable, pin grid array, or any of various other types.

A package substrate 210 having multiple layers allows interconnects 250 within the package substrate 210. This provides more flexibility with designing the 5 layouts of the conductive pads 230 of the opto-electronic substrate 205 and the conductive strips 234 of the package substrate 210. Multiple layers also assists with heat dissipation.

An electrical controller 260 may be coupled to the opto-electronic device 200 to provide control of the electrical inputs to the opto-electronic device 200. In one 10 embodiment the electrical controller 260 and the opto-electronic device 200 are both surface mounted to a circuit board 220, and the electrical coupling between the electrical controller 260 and the opto-electronic device 200 are made through interconnects 262 within the circuit board 220.

Returning to Figure 1, in an alternate embodiment, an electrical controller 15 300 may be integrated onto the package substrate 150. The electrical controller die may be coupled to the electrical strips either via traces on the package substrate 150 or through a multilayer interconnects within the package substrate 150.

Thus, an opto-electronic device coupled to a package substrate via solder 20 bumps is disclosed. However, the specific embodiments and methods described herein are merely illustrative. For example, although a TOS with two heating elements was described, any number of heating elements could be used with the disclosed architecture. Numerous modifications in form and detail may be made

without departing from the scope of the invention as claimed below. The invention is limited only by the scope of the appended claims.

100-200-300-400-500-600-700-800-900